

a variable resistor element, provided between the dividing point of said divider circuit and the control terminal of said amplifying element, which comprise said brightness control circuit.

8. (Amended) The power supply circuit according to claim 7, wherein said divider circuit comprises:

a resistor having a terminal connected to said input power supply; and
a Zener diode having a cathode connected to said resistor and having an anode connected to ground.

9. (Amended) The power supply circuit according to claim 2, wherein said amplifying elements are bipolar transistors.

10. (Amended) The power supply circuit according to claim 2, wherein the impedance of said impedance element is within a range of 40 K Ω to 50 k Ω .

11. (Amended) The power supply circuit according to claim 3, wherein said diodes of said diode group are silicon diodes.

REMARKS

By the present Amendment, Applicants amend claims 1-11 to more appropriately define the present invention. In accordance with the requirements of 37 C.F.R. § 1.121(c)(1), Applicants provide a marked-up version of the amended claims in an attached Appendix. No new matter has been added by these amendments. Claims 1-18 remain pending.

PATENT
Customer No. 22,852
Application No. 09/492,789
Filed: January 28, 2000
Attorney Docket No. 1165.0770-00

In the Final Office Action, the Examiner rejected claims 1, 7-10, and 18 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,663,743 to *Fujii et al.*, in view of U.S. Patent No. 3,956,661 to *Sakamoto et al.* and U.S. Patent No. 4,621,260 to *Suzuki et al.*, claims 11 and 12 were rejected under 35 U.S.C. §103(a) as unpatentable over *Fujii*, *Sakamoto*, and *Suzuki*, and further in view of *The Electrical Engineering Handbook*, CRC Press, 1993; claims 2-4 and 14-15 were rejected under 35 U.S.C. §103(a) as unpatentable over *Fujii*, *Sakamoto*, and *Suzuki*, and further in view of U.S. Patent No. 6,121,943 to *Nishioka et al.*; claims 5 and 6 were rejected under 35 U.S.C. §103(a) as unpatentable over *Fujii*, *Sakamoto*, and *Suzuki*, and further in view of U.S. Patent No. 6,236,394 to *Ikeda*; claim 13 was rejected under 35 U.S.C. §103(a) as unpatentable over *Fujii*, *Sakamoto*, and *Suzuki*, as applied to claim 1, and further in view of U.S. Patent No. 5,473,289 to *Ishizaki et al.*; claim 16 was rejected under 35 U.S.C. §103(a) as unpatentable over *Fujii*, *Sakamoto*, *Suzuki*, and *Nishioka*, as applied to claim 2, and further in view of *The Electrical Engineering Handbook*. Finally, claim 17 was rejected under 35 U.S.C. §103(a) as unpatentable over *Fujii*, *Sakamoto*, *Suzuki*, and *Nishioka*, as applied to claim 2, and further in view of *Ishizaki*.

Applicants respectfully disagree with the Examiner's arguments and conclusions and respectfully traverse the 35 U.S.C. §103(a) rejections for the following reasons.

A *prima facie* case of obviousness has not been made, since the Examiner does not show that all the elements of Applicants' claims are met in the cited

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N.W.
WASHINGTON, DC 20005
202-408-4000

references, and does not show that there is any suggestion or motivation to modify the cited references to result in the claimed invention nor a reasonable expectation of success in doing so. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." See M.P.E.P. §2143 (8th Ed. 2001). The Examiner does not show that all the elements of Applicants' claims are met in the cited references, taken alone or in combination, and does not show that there is any suggestion or motivation to modify the cited references to result in the claimed invention, or any reasonable expectation of success from so doing.

Independent claim 1 is directed to a power supply circuit, which includes, *inter alia*, "a scan driver power circuit for supplying a scan driver voltage to a scan driver for scanning a liquid crystal display device, and which has a data driver power circuit for supplying a data driver voltage to a data driver for sending display data to said liquid crystal display device, comprising: a brightness control circuit ...; a voltage regulation circuit...; and a temperature compensation circuit." Indeed, neither *Fujii*, nor *Sakamoto*, nor *Suzuki* teaches or suggests at least a power supply circuit having a scan driver power circuit, and a data driver power circuit comprising a brightness control circuit, a voltage regulation circuit, and a temperature compensation circuit. *Fujii*, for example, does not even mention such a feature as a temperature compensation circuit. Nor does *Fujii* disclose a brightness control circuit. Similarly, *Sakamoto* and *Suzuki* do not teach temperature compensation circuit or a brightness control circuit. Therefore, the obviousness rejection is improper and must be withdrawn.

PATENT
Customer No. 22,852
Application No. 09/492,789
Filed: January 28, 2000
Attorney Docket No. 1165.0770-00

In summary, Applicants have demonstrated above that the Examiner has not shown all recitations of Applicants' claimed invention are taught or suggested by all the cited references taken alone or in combination. Thus, Applicants submit that the Examiner's reliance on *Fujii*, *Sakamoto*, and *Suzuki* fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a) of claim 1.

Therefore, Applicants submit that independent claim 1 is allowable. In addition, dependent claims 2-18 are also allowable at least by virtue of their dependence from allowable base claim 1. Therefore, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 103(a) rejections.

In view of the foregoing, Applicants submit that the rejections of claims 1-18 are improper and should be withdrawn. Applicants submit that pending claims 1-18 are in condition for allowance.

If there are any fees due under 37 C.F.R. § 114, which are not enclosed, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: December 31, 2002

By: Arthur S. Garrett Reg No 24,014
for Reg. No. 20,338

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N.W.
WASHINGTON, DC 20005
202-408-4000



PATENT
Customer No. 22,852
Application No. 09/492,789
Filed: January 28, 2000
Attorney Docket No. 1165.0770-00

APPENDIX TO AMENDMENT OF DECEMBER 31, 2002
VERSION WITH MARKINGS TO SHOW CHANGES MADE

AMENDMENTS TO THE CLAIMS

Please amend claims 1-11 as follows:

1. (Twice Amended) A power supply circuit, which has a scan driver power circuit for supplying a scan driver [drive] voltage to a scan driver for scanning a liquid crystal display device, and which has a data driver power circuit for supplying a data driver [drive] voltage to a data driver for sending display data to said liquid crystal display device, [said data driver power circuit] comprising:

[an input power supply serving as a universal power supply therefore;
an amplifying element having an input terminal connected to said input power supply, and having a control terminal, and an output terminal from which the data driver power voltage is outputted;

an electric current limiting resistor having a first terminal connected to said input power supply, and having a second terminal connected to said control terminal of said amplifying element;

a diode group including a plurality of series-connected diodes wherein a cathode terminal of a first diode is connected to ground and an anode terminal of a last diode is connected to said control terminal of said amplifying element, and each other diode in the series having a cathode terminal connected to an anode terminal of the preceding diode; and

LAW OFFICES

FINNEMAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N.W.
WASHINGTON, DC 20005
202-408-4000

a capacitor having a first terminal connected to said output terminal of said amplifying element, and a second terminal connected to ground.]

a brightness control circuit, provided in said scan driver power circuit, for controlling brightness of said liquid crystal display device by changing the voltage level of said scan driver voltage;

a voltage regulation circuit, provided in said data driver power circuit, for regulating the voltage level of said data driver voltage supplied to said liquid crystal display device to a predetermined value; and

a temperature compensation circuit, provided in said data driver power circuit, for compensating a temperature characteristic of said liquid crystal display device by changing the voltage level of said data driver voltage.

2. (Amended) The power supply circuit according to claim 1, wherein said [scan] data driver power circuit further comprising [comprises]:

an input power supply serving as a universal power supply therefore [therefor];
an amplifying element having an input terminal connected to said input power supply, and having a control terminal and an output terminal from which the data driver power voltage is outputted; and

[a divider circuit, provided between said input power supply and the ground, for setting an upper limit value of a voltage applied to said control terminal of said amplifying element of said scan driver power circuit; and

a variable resistor having a resistance variation terminal connected to said control terminal of said amplifying element, said variable resistor being operative to vary a voltage appearing at said output terminal of said amplifying element by changing a voltage applied to said control terminal of said amplifying element.]

an impedance element connected between said input power circuit and said control terminal of said amplifying element, said voltage regulation circuit and said temperature compensation circuit being connected to said control terminal of said amplifying element.

3. (Amended) The power supply circuit according to claim 2, wherein [said divider circuit comprises:] said voltage regulation circuit and said temperature compensation circuit comprise a diode group including a plurality of series-connected diodes connected between said control terminal of said amplifying element and ground.

[a resistor having a terminal connected to said input power supply; and a Zener diode having a cathode connected to said resistor and having an anode connected to the ground.]

4. (Amended) The power supply circuit according to claim 3, wherein [a terminal of said variable resistor is] said series-connected diodes each have a cathode terminal connected to said [cathode of said Zener diode.] control terminal of said amplifying element and an anode terminal connected to the ground respectively.

5. (Amended) The power supply circuit according to claim 3 [1], wherein the number of diodes of said diode group is determined from the sum of the voltage

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

PATENT
Customer No. 22,852
Application No. 09/492,789
Filed: January 28, 2000
Attorney Docket No. 1165.0770-00

drop of each diode being approximately equal to said data driver voltage. [data drive voltage is within a range of a voltage which is lower than a threshold voltage of a liquid crystal used in said liquid crystal display device by 20 % of the threshold voltage to a voltage that is higher than the threshold voltage thereof by 20 % of the threshold voltage.]

6. (Amended) The power supply circuit according to claim 5 [1], wherein the number of diodes of said diode group is seven. [data drive voltage is within a range of 20% lower than a peak to peak voltage of a signal to 20% higher than a peak to peak voltage of a signal, which is inputted to said data driver.]

7. (Amended) The power supply circuit according to claim 1, wherein said scan driver power circuit further comprising:

an input power supply serving as a universal power supply therefor;
an amplifying element having an input terminal connected to said input power supply, and having a control terminal and an output terminal from which the data driver power voltage is outputted;

a divider circuit, provided between said input power supply and the ground, for setting a voltage applied to said control terminal of said amplifying element; and

a variable resistor element, provided between the dividing point of said divider circuit and the control terminal of said amplifying element, which comprise said brightness control circuit. [the number of diodes of said diode group is 7.]

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

PATENT
Customer No. 22,852
Application No. 09/492,789
Filed: January 28, 2000
Attorney Docket No. 1165.0770-00

8. (Amended) The power supply circuit according to claim 7 [1], wherein said divider circuit comprises:

a resistor having a terminal connected to said input power supply; and
a Zener diode having a cathode connected to said resistor and having an anode
connected to ground. [diodes of said diode group are silicon diodes.]

9. (Amended) The power supply circuit according to claim 1 2, wherein said amplifying elements are bipolar transistors. [resistance of said current limiting resistor is within a range of 40 k Ω to 50 k Ω .]

10. (Amended) The power supply circuit according to claim 2 [1], wherein the impedance of said impedance element is within a range of 40 K Ω to 50 k Ω . [said amplifying elements are bipolar transistors.]

11. (Amended) The power supply circuit according to claim 3 [1], wherein said diodes of said diode group are silicon diodes. [amplifying elements are field effect transistors.]

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com